APPARATUS AND METHOD FOR DELAY MATCHING OF FULL AND DIVIDED CLOCK SIGNALS

ABSTRACT OF THE DISCLOSURE

A transition delay matching circuit in which the transition delay of the divided clock signal is substantially the same as the transition delay of the reference clock signal. The transition delay of the divided clock signal is adjusted by reducing the steady state amplitude of the divided clock signal. Apparatuses and methods for matching the transition delays of the divided clock signal and the reference clock signal are disclosed.